3MHz Dual Step-Down Converters and Dual Low-Input LDOs with I²C Compatible Interface

ISL9305

The ISL9305 is an integrated mini Power Management IC (mini-PMIC) ideal for applications of powering low-voltage microprocessor or multiple voltage rails with battery as input sources, such as a single Li-ion or Li-Polymer. ISL9305 integrates two high-efficiency 3MHz synchronous step-down converters (DCD1 and DCD2) and two low-input, low-dropout linear regulators (LDO1 and LDO2).

The 3MHz PWM switching frequency allows the use of very small external inductors and capacitors. Both step-down converters can enter skip mode under light load conditions to further improve the efficiency and maximize the battery life. For noise sensitive applications, they can also be programmed through I²C interface to operate in forced PWM mode regardless of the load current condition. The I²C interface supports on-the-fly slew rate control of the output voltage from 0.825V to 3.6V at 25mV/step size for dynamic power saving. Each step-down converter can supply up to 800mA load current. The default output voltage can be set from 0.8V to V_{IN} using external feedback resistors on the adjustable version, or the ISL9305 can be ordered in factory pre-set voltage options from 0.9V to 3.6V in 50mV step.

The ISL9305 also provides two 300mA low dropout (LDO) regulators. The input voltage range is 1.5V to 5.5V allowing them to be powered from one of the on-chip step-down converters or directly from the battery. The default LDO power-up output comes with factory pre-set fixed output voltage options between 0.9V to 3.3V.

The ISL9305 is available in a 4mmx4mm 16 Ld TQFN package.

Related Literature

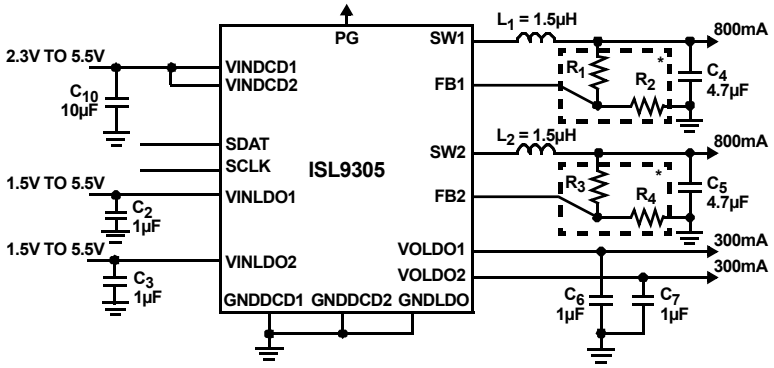
- ISL9305H Data Sheet
- AN1564 "ISL9305 and ISL9305H Evaluation Boards"

Features

- Dual 800mA, Synchronous Step-down Converters and Dual 300mA, General-purpose LDOs
- Input Voltage Range
  - DCD1/DCD2 . . . . . 2.3V to 5.5V
  - LDO1/LDO2 . . . . . 1.5V to 5.5V
- 400kb/s I²C-bus Series Interface Transfers the Control Data Between the Host Controller and the ISL9305
- Adjustable Output Voltage
  - VODCD1/VODCD2 . . . . . 0.8V to V_{IN}
- Fixed Output I²C Programmability
  - At 25mV/Step . . . . . 0.825V to 3.6V
- LDO1/LDO2 Output Voltage I²C Programmability
  - At 50mV/Step . . . . . 0.9V to 3.6V
- 50µA I_Q (Typ) with DCD1/DCD2 in Skip Mode; 20µA I_Q (Typ) for each Enabled LDO
- On-the-fly I²C Programming of DC/DC and LDO Output Voltages
- DCD1/DCD2 I²C Programmable Skip Mode Under Light Load or Forced Fixed Switching Frequency PWM Mode
- Small, Thin, 4mmx4mm TQFN Package

Applications

- Cellular Phones, Smart Phones
- PDAs, Portable Media Players, Portable Instruments
- Single Li-ion/Li-Polymer Battery-Powered Equipment
- DSP Core Power



*Only for adjustable output version. For fixed output version, directly connect the FB pin to the output of the buck converter.

FIGURE 1. TYPICAL APPLICATION DIAGRAM

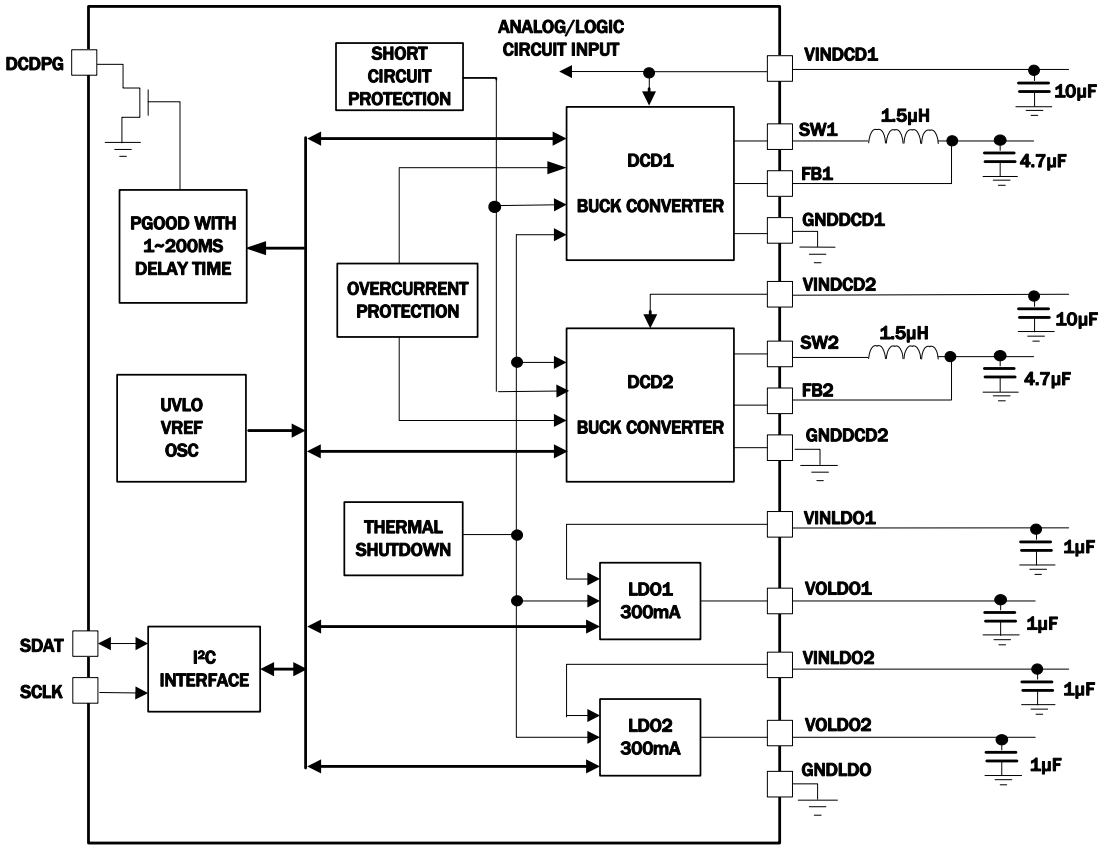
TABLE 1. TYPICAL APPLICATION PART LIST

PARTS	DESCRIPTION	MANUFACTURER	PART NUMBER	SPECIFICATIONS	SIZE
L1, L2	Inductor	Sumida	CDRH2D14NP-1R5	1.5µH/1.80A/50mΩ	3.0mmx3.0mmx1.55mm
C1	Input capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V	0805
C2, C3	Input capacitor	Murata	GRM185R60J105KE26D	1µF/6.3V	0603
C4, C5	Output capacitor	Murata	GRM219R60J475KE01D	4.7µF/6.3V	0805
C6, C7	Output capacitor	Murata	GRM185R60J105KE26D	1µF/6.3V	0603
R1, R2, R3, R4	Resistor	Various		1%, SMD, 0.1Ω	0603

NOTE:

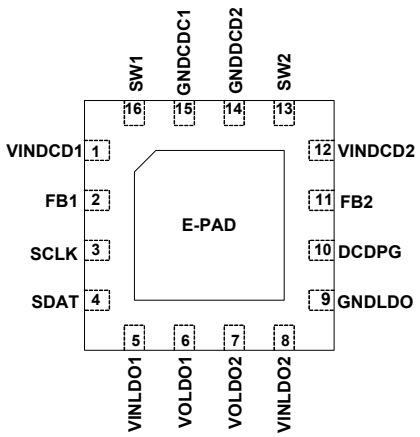
1. C4 and C5 are 10µF/6.3V for VODCD less than 1V.

Block Diagram



Pin Configuration

ISL9305
(16 LD 4x4 TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER (TQFN)	NAME	DESCRIPTION
1	VINDCD1	Input voltage for buck converter DCD1 and it also serves as the power supply pin for the whole internal digital/ analog circuits.
2	FB1	Feedback pin for DCD1, connect external voltage divider resistors between DCDC1 output, this pin and ground. For fixed output versions, connect this pin directly to the DCD1 output.
3	SCLK	I^2C interface clock pin.
4	SDAT	I^2C interface data pin.
5	VINLDO1	Input voltage for LDO1.
6	VOLDO1	Output voltage of LDO1.
7	VOLDO2	Output voltage of LDO2.
8	VINLDO2	Input voltage for LDO2.
9	GNDLDO	Power ground for LDO1 and LDO2.
10	DCDPG	The DCDPG pin is an open-drain output to indicate the state of the DCD1/DCD2 output voltages. When both DCD1 and DCD2 are enabled, the output is released to be pulled high by an external pull-up resistor if both converter voltages are within the power-good range. The pin will be pulled low if either DCD is outside their range. When only one DCD is enabled, the state of the enabled DCD's output will define the state of the DCDPG pin. The DCDPG state can be programmed for a delay of up to 200ms before being released to rise high. The programming range is 1ms~200ms through the I^2C interface.
11	FB2	Feedback pin for DCD2, connect external voltage divider resistors between DCD2 output, this pin and ground. For fixed output versions, connect this pin directly to the DCD2 output.
12	VINDCD2	Input voltage for buck converter DCD2.
13	SW2	Switching node for DCD2, connect to one terminal of the inductor.
14	GNDDCD2	Power ground for DCD2.
15	GNDDCD1	Power ground for DCD1.
16	SW1	Switching node for DCD1, connect to one terminal of the inductor.
E-pad	E-pad	Exposed Pad. Connect to system ground.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	FBSEL DCD1 (V)	FBSEL DCD2 (V)	SLV LDO1 (V)	SLV LDO2 (V)	TEMP. RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL9305IRTAANLZ-T	9305I AANLZ	Adj	Adj	3.3	2.9	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTBCNLZ-T	9305I BCNLZ	1.5	1.8	3.3	2.9	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTBFNCZ-T	9305I BFNCZ	1.5	2.5	3.3	1.8	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTWBNLZ-T	9305I WBNLZ	1.2	1.5	3.3	2.9	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTWCLBZ-T	9305I WCLBZ	1.2	1.8	2.9	1.5	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTWCNLZ-T	9305I WCNLZ	1.2	1.8	3.3	2.9	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTWCNYZ-T	9305I WCNYZ	1.2	1.8	3.3	0.9	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTWLNCZ-T	9305I WLNCZ	1.2	2.9	3.3	1.8	-40 to +85	16 Ld TQFN	L16.4x4G
ISL9305IRTAANLZEV1Z	Evaluation Board							
ISL9305IRTBCNLZEV1Z	Evaluation Board							
ISL9305IRTBFNCZEV1Z	Evaluation Board							
ISL9305IRTWBNLZEV1Z	Evaluation Board							
ISL9305IRTWCLBZEV1Z	Evaluation Board							
ISL9305IRTWCNLZEV1Z	Evaluation Board							
ISL9305IRTWCNYZEV1Z	Evaluation Board							
ISL9305IRTWLNCZEV1Z	Evaluation Board							

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9305. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (Refer to ground)

SW1, SW2 . . . . . -1.5V to 6.5V
FB1, FB2 . . . . . -0.3V to 3.6V
GNDDCD1, GNDDCD2, GNDLDO . . . . . -0.3V to 0.3V
All other pins . . . . . -0.3V to 6.5V
ESD Ratings
Human Body Model (Tested per JESD22-A114F) 3.5kV
Machine Model (Tested per JESD22-A115-A) 225V
Charged Device Model (Tested per JESD22-C101D) 2.2kV
Latch Up (Tested per JESD78B, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TQFN Package (Notes 4, 5)	40.2	5

Maximum Junction Temperature Range . . . . . -40°C to +150°C
Recommended Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VINDCD1 . . . . . 2.3V to 5.5V
VINDCD2 . . . . . 2.3V to VINDCD1
VINLDO1 and VINLDO2 . . . . . 1.5V to VINDCD1
DCD1 and DCD2 Output Current . . . . . 0mA to 800mA
LDO1 and LDO2 Output Current . . . . . 0mA to 300mA
Operating Ambient Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, VINDCD1 = 3.6V, VINDCD2 = 3.3V. For LDO1 and LDO2, VINLDOx = VOLDOx + 0.5V to 5.5V with VINLDOx always no higher than VINDCD1, $L_1 = L_2$ = 1.5µH, C_1 = 10µF, $C_4 = C_5$ = 4.7µF, $C_2 = C_3 = C_6 = C_7$ = 1µF, I_{OUT} = 0A for DCD1, DCD2, LDO1 and LDO2 (see Figure 1 on page 1 for more details). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
VINDCD1, VINDCD2 Voltage Range			**2.3**	-	**5.5**	V
VINDCD1, VINDCD2 Undervoltage Lockout Threshold	V_{UVLO}	Rising	-	2.2	**2.3**	V
		Falling	**1.9**	2.1	-	V
Quiescent Supply Current on VINDCD1	I_{VIN1}	Only DCD1 enabled, no load and no switching on DCD1	-	40	**60**	µA
	I_{VIN2}	Only DCD1 and LDO1 enabled, with no load and no switching on DCD1	-	65	**95**	µA
	I_{VIN3}	Both DCD1 and DCD2 enabled, no load and no switching on both DCD1 and DCD2	-	50	**75**	µA
	I_{VIN4}	Only LDO1 and LDO2 enabled	-	75	**100**	µA
	I_{VIN5}	DCD1, DCD2, LDO1 and LDO2 are enabled, with no load and no switching on both DCD1 and DCD2	-	100	**130**	µA
	I_{VIN6}	Only one DCD in forced PWM mode, no load	-	4	**7.5**	mA
Shutdown Supply Current	I_{SD}	VINDCD1 = 5.5V, DCD1, DCD2, LDO1 and LDO2 are disabled through I^2C interface, VINDCD1 = 4.2V	-	0.15	**5**	µA
Thermal Shutdown			-	155	-	°C
Thermal Shutdown Hysteresis			-	30	-	°C
DCD1 AND DCD2						
FB1, FB2 Regulation Voltage	V_{FB}		**0.785**	0.8	**0.815**	V
FB1, FB2 Bias Current	I_{FB}	FB = 0.75V	-	0.001	-	µA
Output Voltage Accuracy		$V_{IN} = V_O$ + 0.5V to 5.5V (minimal 2.3V), 1mA load	**-3**	-	**+3**	%
Line Regulation		$V_{IN} = V_O$ + 0.5V to 5.5V (minimal 2.3V)	-	0.1	-	%/V
Maximum Output Current			**800**	-	-	mA

Electrical Specifications Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, VINDCD1 = 3.6V, VINDCD2 = 3.3V. For LDO1 and LDO2, VINLDOx = VOLDOx + 0.5V to 5.5V with VINLDOx always no higher than VINDCD1, $L_1 = L_2$ = 1.5µH, C_1 = 10µF, $C_4 = C_5$ = 4.7µF, $C_2 = C_3 = C_6 = C_7$ = 1µF, I_{OUT} = 0A for DCD1, DCD2, LDO1 and LDO2 (see Figure 1 on page 1 for more details). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
P-Channel MOSFET ON-resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.14	**0.2**	Ω
		V_{IN} = 2.3V, I_O = 200mA	-	0.24	**0.40**	Ω
N-Channel MOSFET ON-resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.11	**0.2**	Ω
		V_{IN} = 2.3V, I_O = 200mA	-	0.18	**0.34**	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}		**1.075**	1.3	**1.6**	A
SW Maximum Duty Cycle			-	100	-	%
SW Leakage Current		V_{IN} = 5.5V	-	0.005	**1**	µA
PWM Switching Frequency	f_S		**2.6**	3.0	**3.4**	MHz
SW Minimum ON-time		VFB = 0.75V	-	70	-	ns
Bleeding Resistor			-	115	-	Ω
PG						
Output Low Voltage		Sinking 1mA, FB1 = FB2 = 0.7V	-	-	**0.25**	V
Rising Delay Time		Based on 1ms programmed nominal delay time	**0.6**	1.1	**1.8**	ms
Falling Delay Time		Based on 1ms programmed nominal delay time	-	30	-	µs
PG Pin Leakage Current		PG = VINDCD1 = VINDCD2 = 3.6V	-	0.005	**0.1**	µA
PG Low Rising Threshold		Percentage of nominal regulation voltage	-	91	-	%
PG Low Falling Threshold		Percentage of nominal regulation voltage	-	87	-	%
PG High Rising Threshold		Percentage of nominal regulation voltage	-	112	-	%
PG High Falling Threshold		Percentage of nominal regulation voltage	-	109	-	%
LDO1 AND LDO2						
VINLDO1, VINLDO2 Supply Voltage		No higher than VINDCD1	**1.5**	-	**5.5**	V
VINLDO1, VINLDO2 Undervoltage Lock-out Threshold	V_{UVLO}	VINDCD1 = 2.3V, Rising	-	1.41	1.46	V
		VINDCD1 = 2.3V, Falling	**1.33**	1.37	-	V
Internal Peak Current Limit			**350**	425	**540**	mA
Dropout Voltage		I_O = 300mA, VO ≤ 2.1V	-	125	**250**	mV
		I_O = 300mA, 2.1V < VO ≤ 2.8V	-	100	**200**	mV
		I_O = 300mA, VO > 2.8V	-	80	**170**	mV
Power Supply Rejection Ratio		I_O= 300mA @ 1kHz, V_{IN} = 3.6V, VO = 2.6V, T_A = +25°C	-	55	-	dB
Output Voltage Noise		V_{IN} = 4.2V, I_O = 10mA, T_A = +25°C, BW = 10Hz to 100kHz	-	45	-	μV_{RMS}

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Theory of Operation

DCD1 and DCD2 Introduction

Both the DCD1 and DCD2 converters on ISL9305 use the peak-current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Both converters are able to supply up to 800mA load current. The default output voltage ranges from 0.8V to 3.6V depending on the factory pre-set configuration and can be programmed via the I^2C interface in the range of 0.825V to 3.6V at 25mV/step with a programmable slew rate. An open-drain DCDPG (DCD Power-Good) signal is also provided to monitor the DCD1 and DCD2 output voltages. Optionally, both DCD1 and DCD2 can be programmed to be actively discharged via an on-chip bleeding resistor (typical 115Ω) when the converter is disabled.

Skip Mode (PFM Mode) for DCD1/DCD2

Under light load condition, the DCD1 and DCD2 can be programmed to automatically enter a pulse-skipping mode to minimize the switching loss by reducing the switching frequency. Figure 2 illustrates the skip mode operation. A zero-cross sensing circuit monitors the current flowing through the SW node for zero crossing. When it is detected to cross zero for 16 consecutive cycles, the regulator enters the skip mode. During the 16 consecutive cycles, the inductor current could be negative. The counter is reset to zero when the sensed current flowing through the SW node does not cross zero during any cycle within the 16 consecutive cycles. Once the converter enters the skip mode, the pulse modulation is controlled by an internal comparator while each pulse cycle remains synchronized to the PWM clock. The P-Channel MOSFET is turned on at the rising edge of the clock and turned off when its current reaches ~20% of the peak current limit. As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle-over-cycle. When the output voltage is sensed to reach 1.5% above its nominal voltage, the P-Channel MOSFET is turned off immediately and the inductor current is fully discharged to zero and stays at zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-Channel MOSFET will be turned on again, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage is sensed to drop below 1.5% of its nominal voltage value as shown in Figure 3.

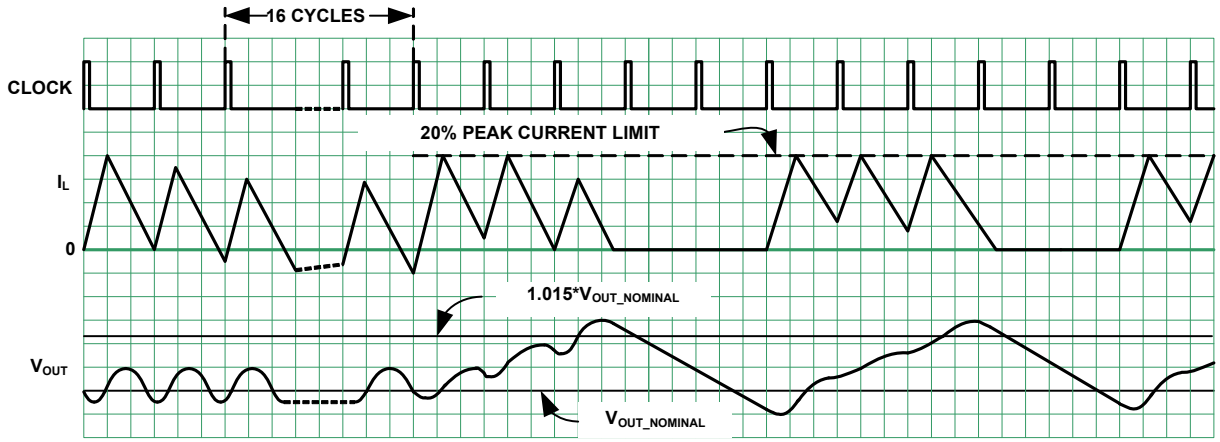


FIGURE 2. SKIP MODE OPERATION WAVEFORMS

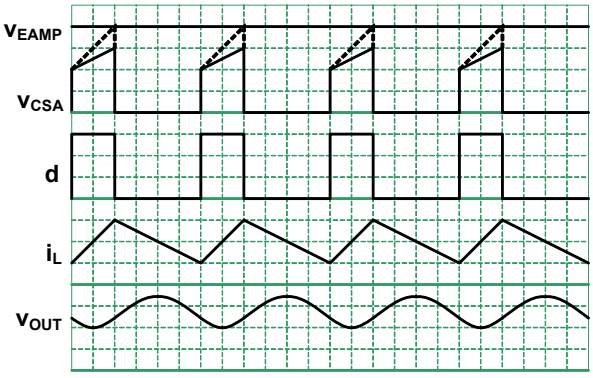


FIGURE 3. PWM OPERATION WAVEFORMS

Soft-Start

The soft-start reduces the in-rush current during the start-up stage. The soft-start block limits the current rising speed so that the output voltage rises in a controlled fashion.

Overcurrent Protection

The overcurrent protection for DCD1 and DCD2 is provided on ISL9305 for when an overload condition occurs. When the current at P-Channel MOSFET is sensed to reach the current limit, the internal protection circuit is triggered to turn off the P-Channel MOSFET immediately.

DCD Short-Circuit Protection

The ISL9305 provides Short-Circuit Protection for both DCD1 and DCD2. The feedback voltage is monitored for output short-circuit protection. When the output voltage is sensed to be lower than a certain threshold, the internal circuit will change the PWM oscillator frequency to a lower frequencies in order to protect the IC from damage. The P-Channel MOSFET peak current limit remains active during this state.

Undervoltage Lock-out (UVLO)

An undervoltage lock-out (UVLO) circuit is provided on ISL9305. The UVLO circuit block can prevent abnormal operation in the event that the supply voltage is too low to guarantee proper operation. The UVLO on VINDCD1 is set for a typical 2.2V with 100mV hysteresis. VINLDO1 and VINLDO2 are set for a typical 1.4V with 50mV hysteresis. When the input voltage is sensed to be lower than the UVLO threshold, the related channel is disabled.

DCDPG (DCD Power-Good)

ISL9305 offers an open-drain Power-Good signal with programmable delay time for monitoring the converters DCD1 and DCD2 output voltages status.

When both DCD1 and DCD2 are enabled and their output voltages are within the power-good window, an internal power-good signal is issued to turn off the open-drain MOSFET so the DCDPG pin voltage can be externally pulled high after a programmed delay time. If either DCD1 or DCD2 output voltages or both of them are not within the power-good window, the DCDPG outputs an open-drain logic low signal after the programmed delay time.

When there is only one DCD converter (either DCD1 or DCD2) is enabled, then the DCDPG only indicates the status of this active DCD converter. For example, if only DCD1 converter is enabled and DCD2 converter is disabled, when DCD1 output is within the power-good window, internal power-good signal will be issued to turn off the open-drain MOSFET so the DCDPG pin voltage is externally pulled high after the programmed delay time. If output voltage of DCD1 is outside the power-good window, the DCDPG outputs an open-drain logic low signal after the programmed delay time. It is similar when only DCD2 is enabled and DCD1 is disabled. When both converters are disabled, DCDPG always outputs the open-drain logic low signal.

Low Dropout Operation

Both DCD1 and DCD2 converters feature the low dropout operation to maximize the battery life. When the input voltage drops to a level that the converter can no longer operate under switching regulation to maintain the output voltage, the P-Channel MOSFET is completely turned on (100% duty cycle). The dropout voltage under such a condition is the product of the load current and the ON-resistance of the P-Channel MOSFET. Minimum required input voltage V_{IN} under such condition is the sum of output voltage plus the voltage drop across the inductor and the P-Channel MOSFET switch.

Active Output Voltage Discharge For DCD1/DCD2

The ISL9305 offers a feature to actively discharge the output voltage of DCD1 and DCD2 via an internal bleeding resistor (typical 115Ω) when the channel is disabled. This feature is enabled by default, thus outputs can be disabled individually through programming the control bit in DCD_PARAMETER register.

Thermal Shutdown

The ISL9305 provides built-in thermal protection function with thermal shutdown threshold temperature set at +155°C with +25°C hysteresis (typical). When the die temperature is sensed to reach +155°C, the regulator is completely shut down and as the temperature is sensed to drop to +130°C (typical), the device resumes normal operation starting from the soft-start.

Board Layout Recommendations

The ISL9305 is a high frequency switching charger and hence the PCB layout is a very important design practice to ensure a satisfactory performance.

The power loop is composed of the output inductor L, the output capacitor C_{OUT}, the SW pin and the PGND pin. It is important to make the power loop as small as possible and the connecting traces among them should be direct, short and wide; the same practice should be applied to the connection of the VIN pin, the input capacitor C_{IN} and PGND.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the voltage feedback trace and other noise sensitive traces away from these noisy traces.

The input capacitor should be placed as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible as well. In addition, a solid ground plane is helpful for a good EMI performance.

The ISL9305 employs a thermal enhanced TQFN package with an exposed pad. The exposed pad should be properly soldered on thermal pad of the board in order to remove heat from the IC. The thermal pad should be big enough for 9 vias as shown in Figure 4.

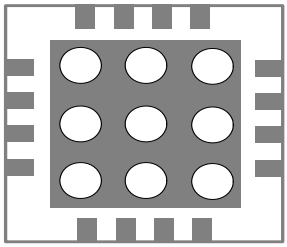


FIGURE 4. EXPOSED THERMAL PAD

I²C Compatible Interface

The ISL9305 offers an I²C compatible interface, using two pins: SCLK for the serial clock and SDAT for serial data respectively. According to the I²C specifications, a pull-up resistor is needed for the clock and data signals to connect to a positive supply. When the ISL9305 and the host use different supply voltages, the pull-up resistors should be connected to the higher voltage rail.

Signal timing specifications should satisfy the standard I²C bus specification. The maximum bit rate is 400kb/s and more details regarding the I²C specifications can be found from Philips.

I²C Slave Address

The ISL9305 serves as a slave device and the 7-bit default chip address is 1101000, as shown in Figure 5 According to the I²C specifications, here the value of Bit 0 determines the direction of the message (“0” means “write” and “1” means “read”).

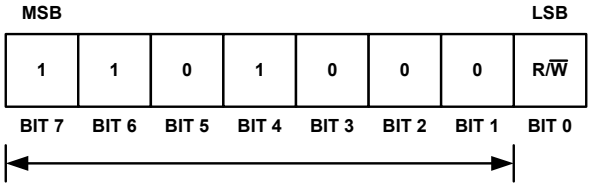


FIGURE 5. I²C SLAVE ADDRESS

I²C Protocol

Figures 6, 7, and 8 show three typical I²C-bus transaction protocols.

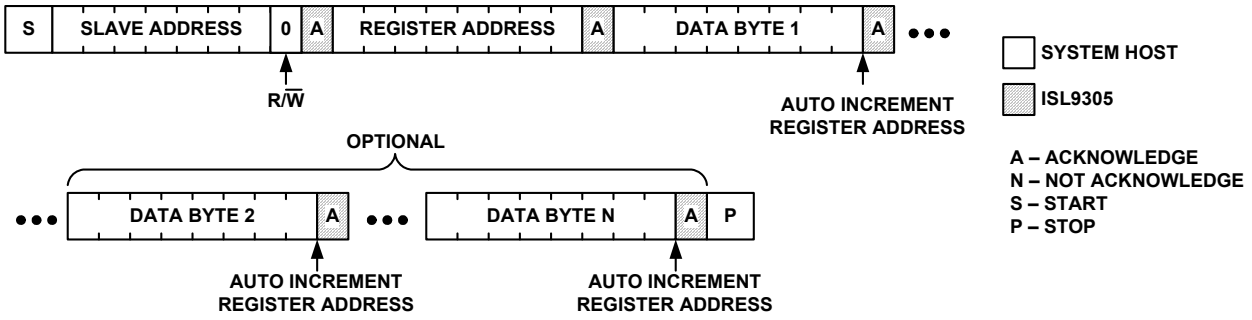


FIGURE 6. I²C WRITE

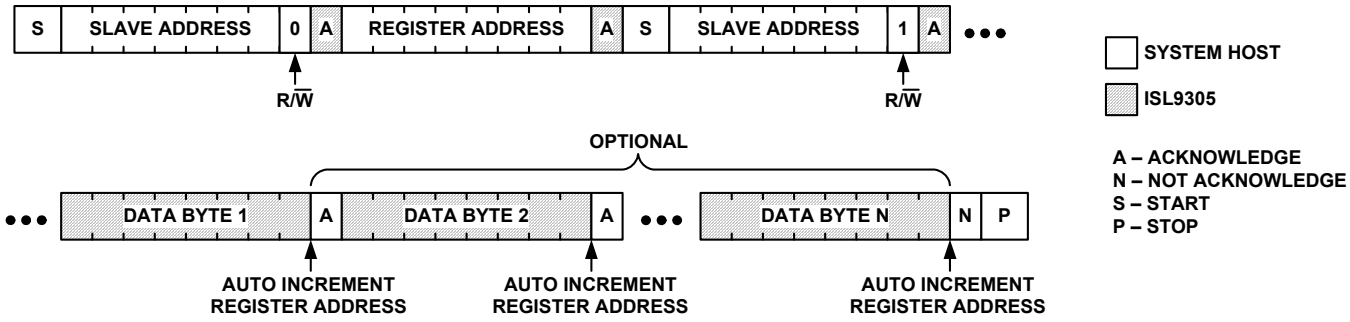


FIGURE 7. I²C READ SPECIFYING REGISTER ADDRESS

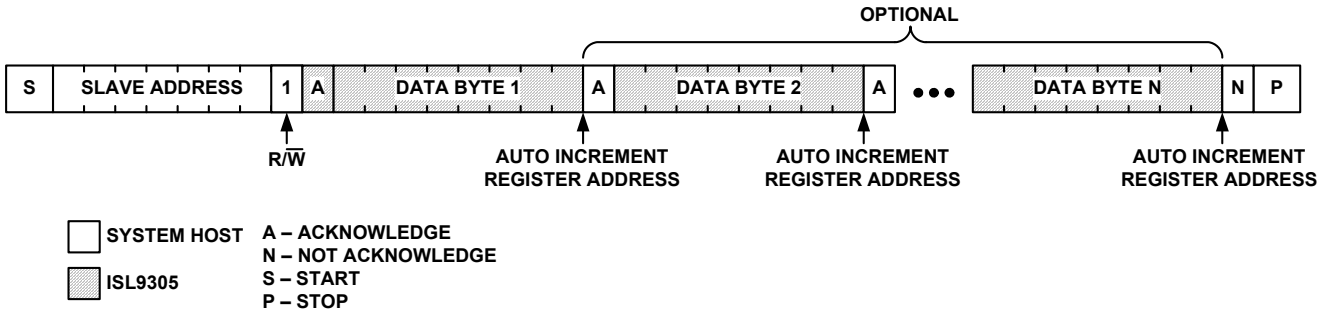


FIGURE 8. I²C READ NOT SPECIFYING REGISTER ADDRESS

I²C Control Registers

All the registers are reset at initial start-up.

DCD OUTPUT VOLTAGE CONTROL REGISTER

DCD1OUT, address 0x00h; DCD2OUT, address 0x01h

TABLE 2. BUCK CONVERTERS OUTPUT VOLTAGE CONTROL REGISTER

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	Reserve	-	0	Refer to Table 3
B6	DCDxOUT-6	R/W	0	
B5	DCDxOUT-5	R/W	0	
B4	DCDxOUT-4	R/W	1	
B3	DCDxOUT-3	R/W	0	Refer to Table 3
B2	DCDxOUT-2	R/W	0	
B1	DCDxOUT-1	R/W	0	
B0	DCDxOUT-0	R/W	0	

TABLE 3. DCD1 AND DCD2 OUTPUT VOLTAGE SETTING

DCDOUT <7:0>	DCD OUTPUT VOLTAGE (V)	DCDOUT <7:0>	DCD OUTPUT VOLTAGE (V)	DCDOUT <7:0>	DCD OUTPUT VOLTAGE (V)	DCDOUT <7:0>	DCD OUTPUT VOLTAGE (V)
00	0.825	20	1.625	40	2.425	60	3.225
01	0.850	21	1.650	41	2.450	61	3.250
02	0.875	22	1.675	42	2.475	62	3.275
03	0.900	23	1.700	43	2.500	63	3.300
04	0.925	24	1.725	44	2.525	64	3.325
05	0.950	25	1.750	45	2.550	65	3.350
06	0.975	26	1.775	46	2.575	66	3.375
07	1.000	27	1.800	47	2.600	67	3.400
08	1.025	28	1.825	48	2.625	68	3.425
09	1.050	29	1.850	49	2.650	69	3.450
0A	1.075	2A	1.875	4A	2.675	6A	3.475
0B	1.100	2B	1.900	4B	2.700	6B	3.500
0C	1.125	2C	1.925	4C	2.725	6C	3.525
0D	1.150	2D	1.950	4D	2.750	6D	3.550
0E	1.175	2E	1.975	4E	2.775	6E	3.575
0F	1.200	2F	2.000	4F	2.800	6F	3.600
10	1.225	30	2.025	50	2.825		
11	1.250	31	2.050	51	2.850		
12	1.275	32	2.075	52	2.875		
13	1.300	33	2.100	53	2.900		
14	1.325	34	2.125	54	2.925		
15	1.350	35	2.150	55	2.950		
16	1.375	36	2.175	56	2.975		
17	1.400	37	2.200	57	3.000		
18	1.425	38	2.225	58	3.025		
19	1.450	39	2.250	59	3.050		
1A	1.475	3A	2.275	5A	3.075		
1B	1.500	3B	2.300	5B	3.100		
1C	1.525	3C	2.325	5C	3.125		
1D	1.550	3D	2.350	5D	3.150		
1E	1.575	3E	2.375	5E	3.175		
1F	1.600	3F	2.400	5F	3.200		

LDO1 AND LDO2 OUTPUT VOLTAGE CONTROL REGISTERS

LDO1OUT, address 0x02h and LDO2OUT, address 0x03h.

TABLE 4. LDOX OUTPUT VOLTAGE CONTROL REGISTERS

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	Reserve	-	0	Refer to Table 5 for output voltage settings
B6	Reserve	-	0	
B5	LDOxOUT-5	R/W	0	
B4	LDOxOUT-4	R/W	0	
B3	LDOxOUT-3	R/W	1	
B2	LDOxOUT-2	R/W	1	
B1	LDOxOUT-1	R/W	0	
B0	LDOxOUT-0	R/W	0	

TABLE 5. LDOX OUTPUT VOLTAGE SETTINGS

LDOOUT <7:0>	LDO OUTPUT VOLTAGE (V)	LDOOUT <7:0>	LDO OUTPUT VOLTAGE (V)	LDOOUT <7:0>	LDO OUTPUT VOLTAGE (V)	LDOOUT <7:0>	LDO OUTPUT VOLTAGE (V)
00	0.90	10	1.70	20	2.50	30	3.30
01	0.95	11	1.75	21	2.55	31	3.35
02	1.00	12	1.80	22	2.60	32	3.40
03	1.05	13	1.85	23	2.65	33	3.45
04	1.10	14	1.90	24	2.70	34	3.50
05	1.15	15	1.95	25	2.75	35	3.55
06	1.20	16	2.00	26	2.80	36	3.60
07	1.25	17	2.05	27	2.85		
08	1.30	18	2.10	28	2.90		
09	1.35	19	2.15	29	2.95		
0A	1.40	1A	2.20	2A	3.00		
0B	1.45	1B	2.25	2B	3.05		
0C	1.50	1C	2.30	2C	3.10		
0D	1.55	1D	2.35	2D	3.15		
0E	1.60	1E	2.40	2E	3.20		
0F	1.65	1F	2.45	2F	3.25		

DCD1 AND DCD2 CONTROL REGISTER

DCD_PARAMETER, address 0x04h

TABLE 6. DCD_PARAMETER REGISTER

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	-	-	0	Reserved
B6	DCD_PHASE	R/W	0	DCD1 and DCD2 PWM switch selection. 0-in phase; 1 to 180° out-of-phase.
B5	DCD2_ULTRA	R/W	0	Ultrasonic feature under PFM mode for DCD2. 0-disabled; 1-enabled.
B4	DCD1_ULTRA	R/W	0	Ultrasonic feature under PFM mode for DCD1. 0-disabled; 1-enabled.
B3	DCD2_BLD	R/W	1	Selection of DCD2 for active output voltage discharge when disabled. 0-disabled; 1-enabled.

TABLE 6. DCD_PARAMETER REGISTER (Continued)

BIT	NAME	ACCESS	RESET	DESCRIPTION
B2	DCD1_BLD	R/W	1	Selection of DCD1 for active output voltage discharge when disabled. 0-disabled; 1-enabled.
B1	DCD2_MODE	R/W	1	Selection on DCD2 of auto PFM/PWM mode (= 1) or forced PWM mode (= 0).
B0	DCD1_MODE	R/W	1	Selection on DCD1 of auto PFM/PWM mode (= 1) or forced PWM mode (= 0).

SYSTEM CONTROL REGISTER

SYS_PARAMETER, address 0x05h

TABLE 7. SYS_PARAMETER REGISTER

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	-	-	0	Reserved
B6	I^2C_EN	R/W	0	I^2C function enable. 0-disabled; 1-enabled
B5	DCDPOR_1	R/W	1	DCDPOR Delay Time Setting, DCDPOR[1:0]: 00 to 1ms 01 to 50ms 10 to 150ms 11 to 200m
B4	DCDPOR_0	R/W	0	
B3	LDO2_EN	R/W	1	LDO2 enable selection. 0-disable, 1-enable.
B2	LDO1_EN	R/W	1	LDO1 enable selection. 0-disable, 1-enable
B1	DCD2_EN	R/W	1	DCD2 enable selection. 0-disable, 1-enable.
B0	DCD1_EN	R/W	1	DCD1 enable selection. 0-disable, 1-enable

DCD OUTPUT VOLTAGE SLEW RATE CONTROL REGISTER

DCD_SRCTL, address 0x06h

TABLE 8.

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	DCD2SR_2	R/W	0	DCD2 Slew Rate Setting, DCD2SR[2:0]: 000 to 0.225mV/µs 001 to 0.45mV/µs 010 to 0.90mV/µs 011 to 1.8mV/µs 100 to 3.6mV/µs 101 to 7.2mV/µs 110 to 14.4mV/µs 111 to 28.8mV/µs
B6	DCD2SR_1	R/W	0	
B5	DCD2SR_0	R/W	1	
B4	Reserve	-	0	Reserved
B3	DCD1SR_2	R/W	0	DCD1 Slew Rate Setting, DCD1SR[2:0]: 000 to 0.225mV/µs 001 to 0.45mV/µs 010 to 0.90mV/µs 011 to 1.8mV/µs 100 to 3.6mV/µs 101 to 7.2mV/µs 110 to 14.4mV/µs 111 to 28.8mV/µs
B2	DCD1SR_1	R/W	0	
B1	DCD1SR_0	R/W	1	
B0	Reserve	-	0	Reserved

Typical Operating Conditions

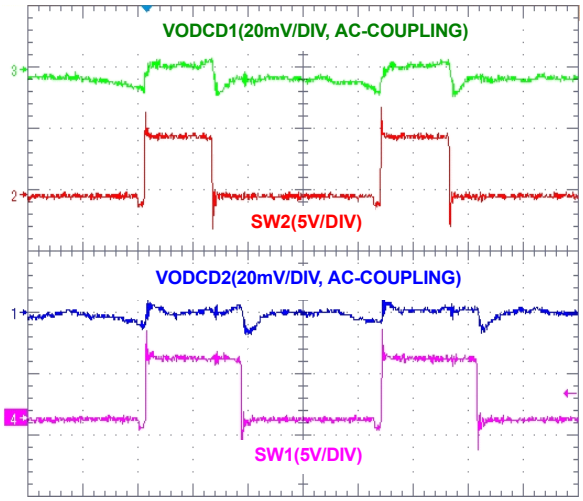


FIGURE 9. DCD OUTPUT VOLTAGE RIPPLE (V_{IN} = 4.2V, FULL LOAD AT DCD1 AND DCD2)

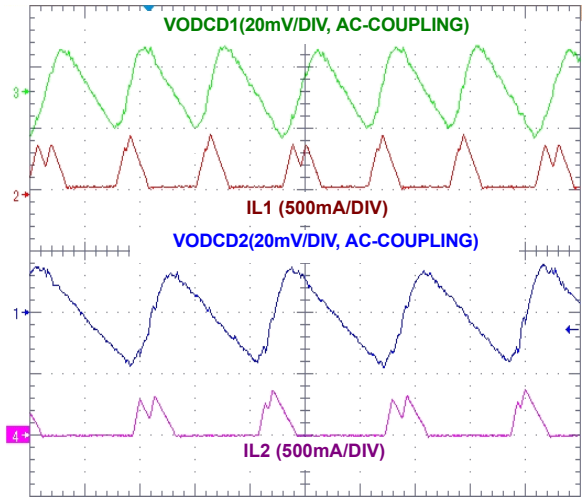


FIGURE 10. DCD OUTPUT VOLTAGE RIPPLE (V_{IN} = 4.2V, PFM MODE)

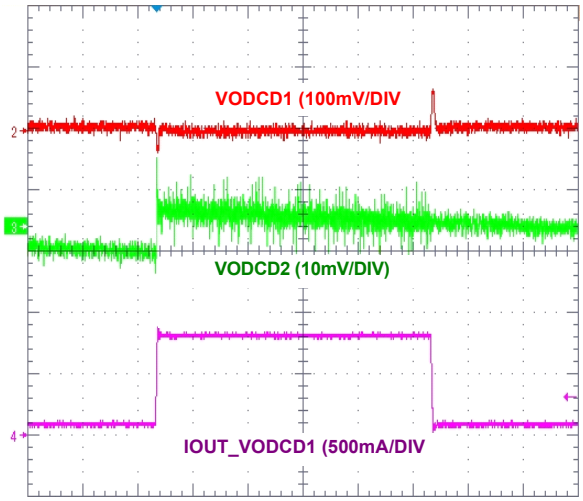


FIGURE 11. DCD OUTPUT TRANSIENT RESPONSE (V_{IN} = 4.2V, LOAD STEP: 80mA TO 800mA)

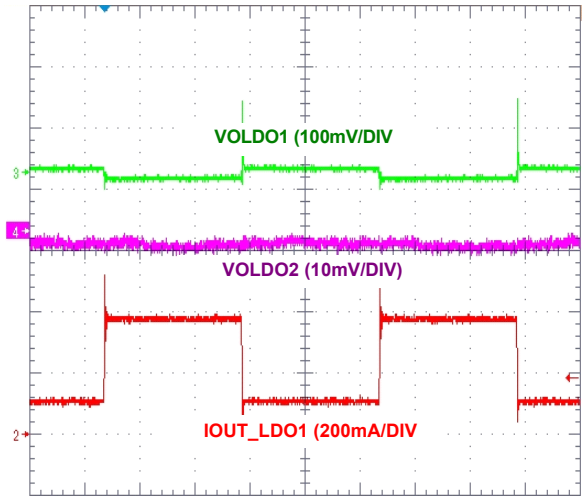


FIGURE 12. LDO OUTPUT TRANSIENT RESPONSE (V_{IN} = 4.2V, STEP LOAD: 30mA TO 300mA)

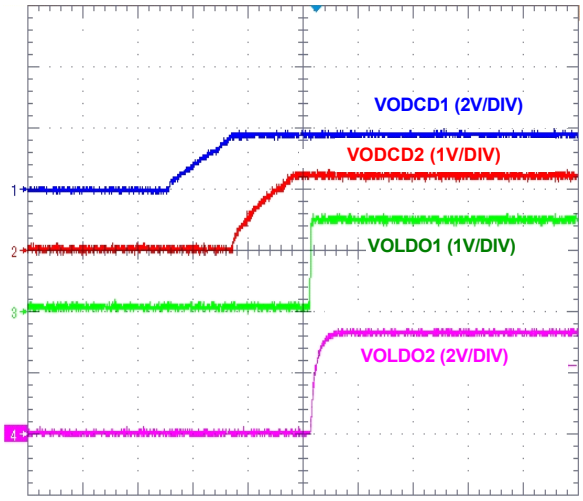


FIGURE 13. START-UP SEQUENCE (V_{IN} = 4.2V, NO LOAD)

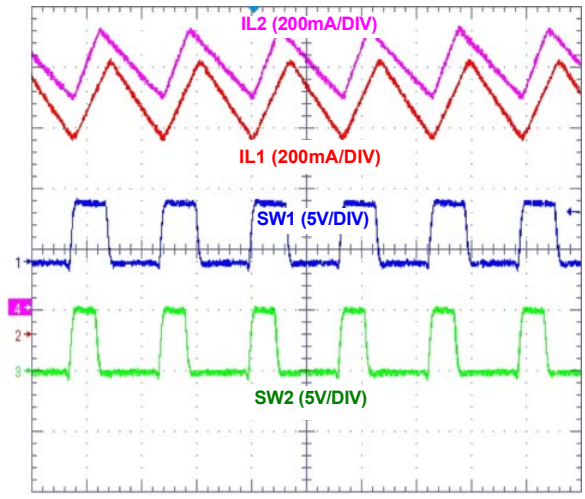


FIGURE 14. DCD1 AND DCD2 SWITCHING WAVEFORM (V_{IN} = 5V, FULL LOAD ON TWO CHANNELS)

Typical Operating Conditions (Continued)

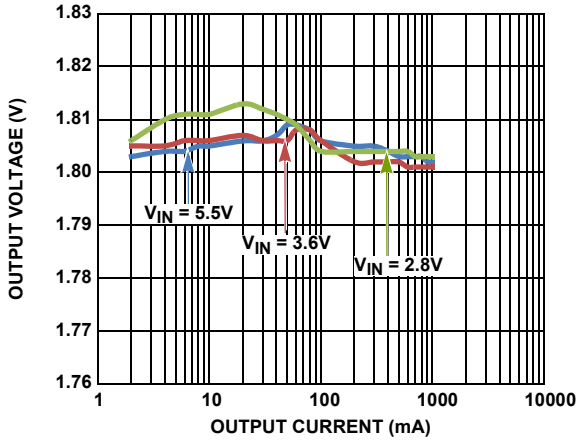


FIGURE 15. DCD OUTPUT VOLTAGE vs LOAD (V_{OUT} = 1.8V, PFM/PWM)

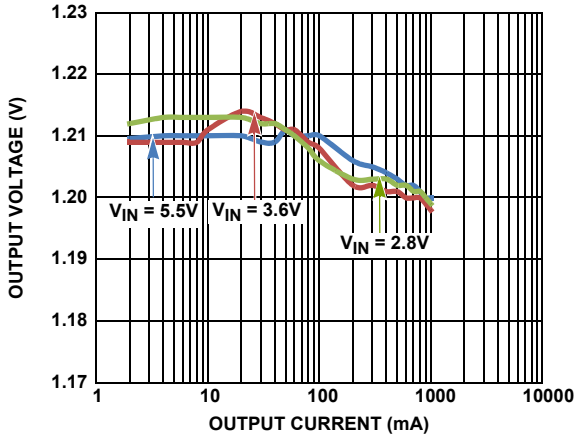


FIGURE 16. DCD OUTPUT VOLTAGE vs LOAD (V_{OUT} = 1.2V, PFM/PWM)

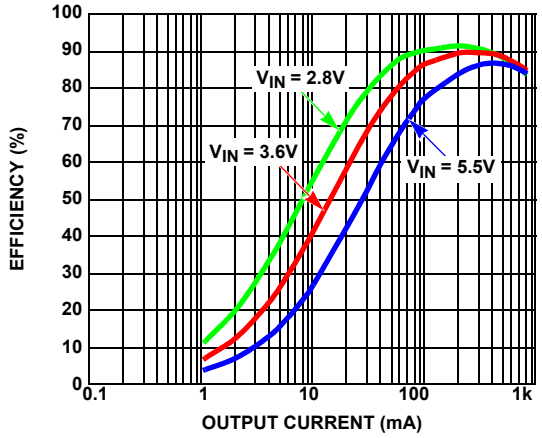


FIGURE 17. EFFICIENCY vs OUTPUT CURRENT (V_{OUT} = 1.8V, FORCED PWM MODE)

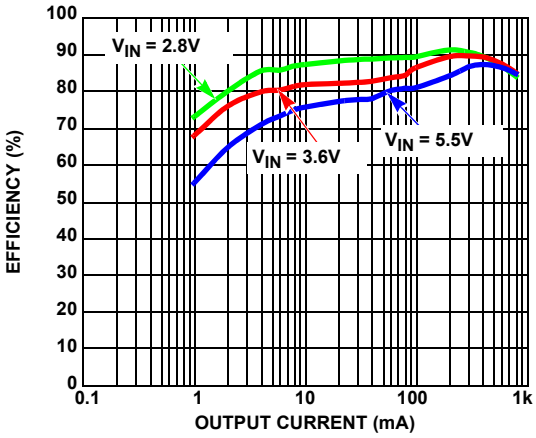


FIGURE 18. EFFICIENCY vs OUTPUT CURRENT (V_{OUT} = 1.8V, PFM TO PWM)

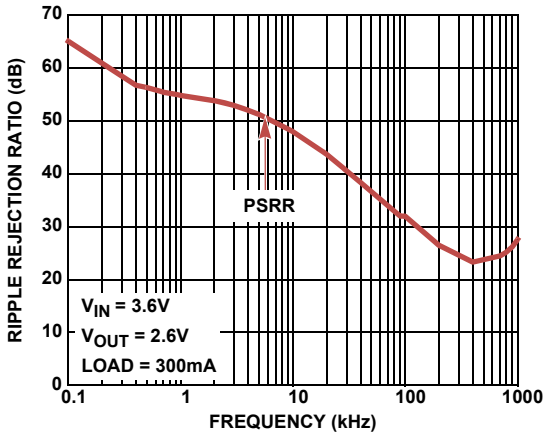


FIGURE 19. RIPPLE REJECTION RATIO vs FREQUENCY

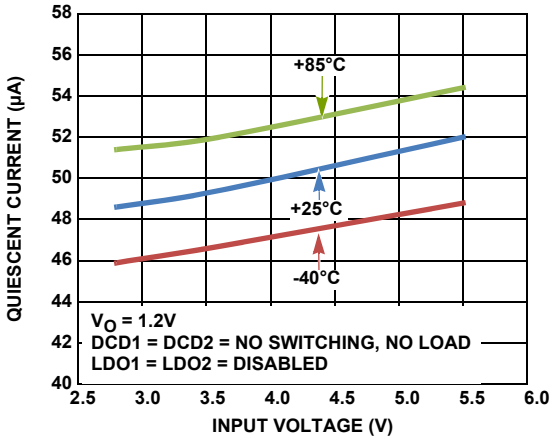


FIGURE 20. QUIESCENT CURRENT vs INPUT VOLTAGE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
February 9, 2015	FN7605.2	page 5, Abs Max Rating, ESD Ratings, change from: Machine Model (Tested per JESD22-A115-A) . . . . . 2.2kV Charged Device Model (Tested per JESD22-C101D) . . . . 225V to: Machine Model (Tested per JESD22-A115-A) . . . . . 225V Charged Device Model (Tested per JESD22-C101D) . . . . 2.2kV page 1 - Changed Related Literature AN1564 title from “ISL9305IRTZEVAL1Z and ISL9305HIRTZEVAL1Z Evaluation Boards” to “ISL9305 and ISL9305H Evaluation Boards” page 1 - Changed “the ISL9305 can be ordered in factory pre-set power-up default voltages in increments of 100mV from 0.9V to 3.6V.” to “the ISL9305 can be ordered in factory pre-set output voltage options from 0.9V to 3.6V in 50mV step.” page 1 Features - Changed “at 50mV/Step.....0.9V to 3.3V” to “50mV/Step.....0.9V to 3.6V” under LDO1/LDO2 output voltage I^2C programmability. page 2 - Change the output capacitor value at VOLDO1 and VOLDO2 from "10µF" to "1µF" in the block diagram. page 4 - Changed Eval Board part numbers in Ordering Information table from “ISL9305IRTBCNLZEV1Z, ISL9305IRTBFNCZEV1Z, ISL9305IRTAANLZEV1Z” to “ISL9305IRTAANLZEV1Z, ISL9305IRTBCNLZEV1Z, ISL9305IRTBFNCZEV1Z, ISL9305IRTWBNLZEV1Z, ISL9305IRTWCLBZEV1Z, ISL9305IRTWCNLZEV1Z, ISL9305IRTWCNYZEV1Z, ISL9305IRTWLNCZEV1Z” page 12 - Removed PCN “Note 7” under Table 8. Changed “111 to reserve for system use” to “111 to 28.8mV/µs. Changed “DCD2” to “DCD1” in line B0 of Table 7.
May 25, 2011	FN7605.1	- Table 8 on page 12 changed 111 description from “to immediate” to “reserved for system use (Note 7).” Added Note to Table 8, which reads "The IC can be damaged when output is programmed from high to low and the slew rate register is set to 111." - Changed ordering information EVAL Board name from ISL9305IRTZEVAL1Z to three separate ones ISL9305IRTBCNLZEV1Z ISL9305IRTBFNCZEV1Z ISL9305IRTAANLZEV1Z - Corrected Theta JA Thermal Information on page 5 for TQFN from 42 to 40.2 - “Electrical Specifications” on page 5: Added "Boldface limits apply over the operating temperature range, -40°C to +85°C." to common conditions. Bolded applicable specs. - Changed “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.” note in Electrical Spec Table on page 6 to “Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.” per Product Line decision. - Changed text under Figure 15, from "VOUT = 1.2V" to "VOUT = 1.8V."
November 8, 2010	FN7605.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

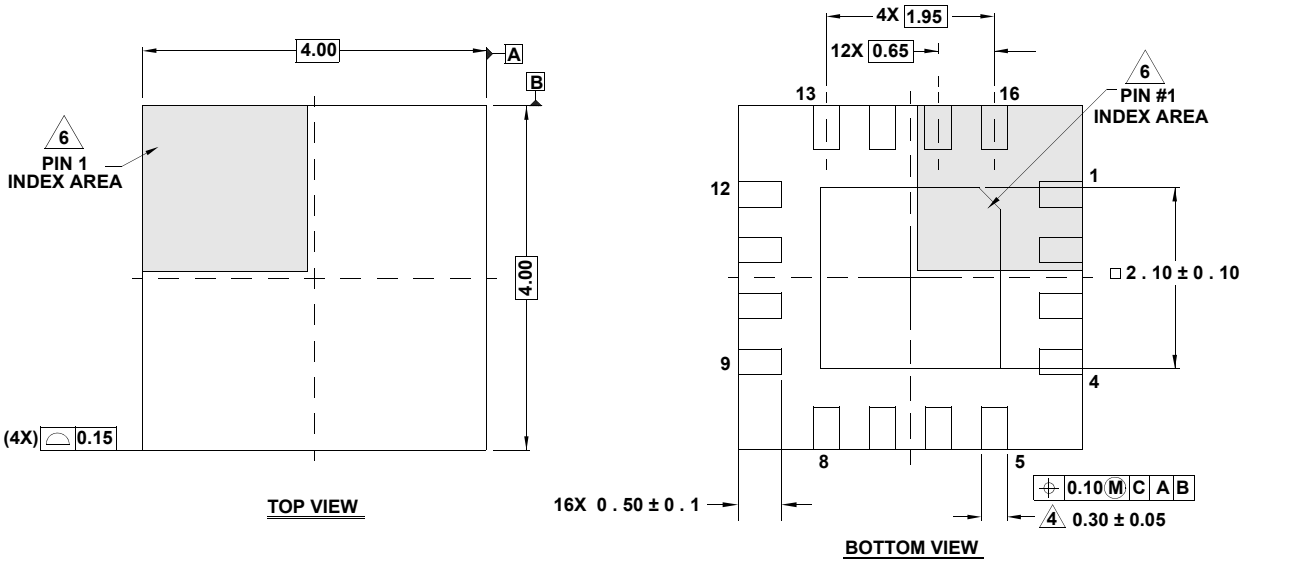
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

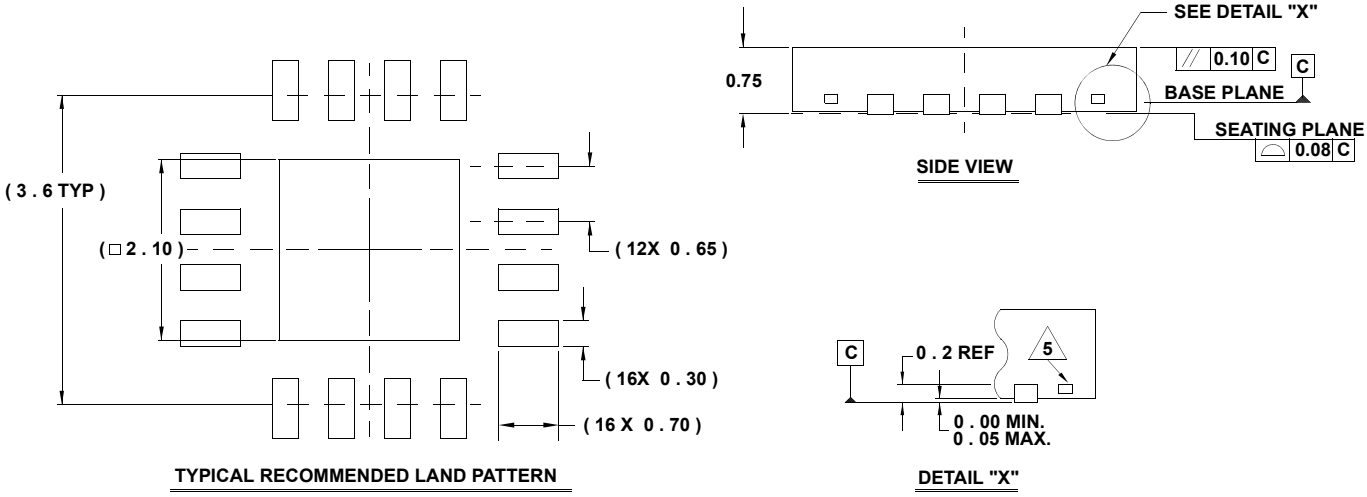
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

L16.4x4G

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 4/10





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO220K.